(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 06084684 A
(43) Date of publication of application: 25.03.1994

(51) Int. Cl H01G 1/14
H01G 4/08

(21) Application number: 04255640
(22) Date of filing: 31.08.1992

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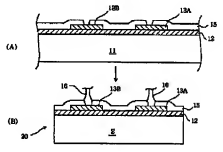
(54) SILICON CHIP CAPACITOR

(57) Abstract:

PURPOSE: To improve high frequency characteristics when a chip capacitor is mounted on a board or the like by arranging both electrodes on one side of the chip capacitor.

CONSTITUTION: A dielectric i.e., an SiO_2 layer 12, is formed on the surface of a silicon chip 2 and polysilicon layers 13A, 13B (electrodes) are provided thereon. Since both lead wires can be led out from one side of the silicon chip 2, routing of wiring pattern can be shortened when the silicon chip capacitor is mounted on a substrate or the like. This constitution prevents high frequency characteristics of circuit from deteriorating.



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CLAIMS

[Claim(s)]
[Claim 1]A laminated silicon chip.
Silicon oxide laminated by the surface or a rear face of this silicon chip.
It is an electrode of a couple at least.
it is the chip type silicon capacitor provided with the above -- the above -- even if small, an electrode of a couple was laminated on the above-mentioned silicon oxide

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application]In this invention, the electrode of a couple is allocated in the square-shaped silicon chip surface via silicon oxide, for example.
Therefore, it is related with the chip type silicon capacitor which can improve the high frequency characteristic at the time of mounting.

[0002]

[Description of the Prior Art]There are some which are shown in JP,2-16708,A as this conventional kind of a chip type silicon capacitor. this silicon capacitor oxidizes the surface of a silicon chip, and forms silicon oxide (SiO2) -- this silicon oxide top -- an electrode -- public funds -- group films (Au etc.) are laminated. This silicon oxide is used as a dielectric layer, and the silicon chip and metal membrane which sandwich this are constituted as an electrode of a couple. That is, if it is in this silicon chip, the electrode is provided in the rear surface of the silicon chip, respectively.

[0003]As for this chip type silicon capacitor, SiO2 which constitutes a dielectric layer is homogeneous, it is a very stable substance without a defect, and those temperature characteristics and a frequency characteristic are extremely excellent. It is easy for thickness to form this dielectric layer thinly with 2 micrometers, and big electric capacity by this can be secured.

[0004]

[Problem(s) to be Solved by the Invention]The electrode of such a couple of a chip type silicon capacitor was provided in the rear surface of the silicon chip, respectively, as mentioned above. For this reason, when it mounts this chip type silicon capacitor in a substrate etc., the circuit pattern of a substrate must be set by the position of two electrodes. For example, if two

circuit patterns are connectable with one field of a chip type silicon capacitor, a circuit pattern must be connected to the rear surface of a chip type silicon capacitor even if it is a case where the circuit pattern concerned can be shortened. As a result, leading about of a circuit pattern became long, the inductance of a circuit pattern and the parasitic capacitance between circuit patterns increased, and the problem that the high frequency characteristic of a circuit got worse had arisen.

[0005]

[Objects of the Invention]Then, an object of this invention is to improve the high frequency characteristic at the time of mounting a chip type capacitor in a substrate etc. by allocating the electrode of a couple in the field of 1 of a chip type silicon capacitor.

[0006]

[Means for Solving the Problem]Such a purpose is attained by following this invention. Namely, in a chip type silicon capacitor which has an electrode of a couple at least in this invention with a laminated silicon chip and silicon oxide (dielectric layer) laminated by the surface or a rear face of this silicon chip, the above -- even if small, an electrode of a couple is laminated on the above-mentioned silicon oxide.

[0007]

[Function]Two electrodes are laminated by silicon oxide in the chip type silicon capacitor concerning this invention. namely, any of two electrodes -- although -- one field of the silicon chip laminates via silicon oxide. Therefore, it becomes possible from one field of a silicon chip to pull out a lead etc. Therefore, since leading about of a circuit pattern can be shortened when it mounts this chip type silicon capacitor in a substrate etc., it becomes possible to prevent the high frequency characteristic of a circuit from getting worse.

[0008]

[Example]The example of this invention is explained in full detail below. Drawing 1 and drawing 2 are the sectional views for explaining the manufacturing process of the chip type silicon capacitor concerning the 1st example of this invention.

[0009]As drawing 2 is shown in (B), the chip type silicon capacitor 20, It has the square-shaped silicon chip 2, a dielectric which consists of SiO two-layer 12 laminated by the surface of this silicon chip 2, and an electrode of the couple which consists of the polysilicon layers 13A and 13B laminated on this SiO two-layer 12.

[0010]And in this invention, the SiO two-layer 12 of the chip type silicon capacitor 20 which is the above-mentioned laminated structure body, and the polysilicon layers 13A and 13B are covered, and the SiO2 film 15 is laminated. The thickness of this SiO2 film 15 presupposes that it is the same as the above-mentioned thickness SiO two-layer [12]. Mounting is presented with such a chip type silicon capacitor 1 of structure as individual electronic parts by welding by pressure electric wires, such as a Dumet wire, to the polysilicon layers 13A and

13B which are electrodes, and closing the periphery with glassware.
[0011]The equivalent circuit of this chip type silicon capacitor 20, As shown in drawing 3, the capacitor C1 expressed with the two capacitors C1, C2, and the resistance R, Expressing the capacitor formed between the polysilicon layer 13A and the silicon chip 2, the capacitor C2 expresses the capacitor formed between the polysilicon layer 13B and the silicon chip 2. The pressure-proofing in this chip type silicon capacitor 20, capacity, etc. are determined by the area (electrode area) of the polysilicon layers 13A and 13B, thickness SiO two-layer [12], etc. And the resistance R expresses the electrical resistance between the portions of the silicon chip 2 which counters the polysilicon layers 13A and 13B. The value of the resistance R can be changed by choosing suitably the concentration of the impurity added to the silicon chip 2. The resistivity of the silicon chip 2 is a 10-ohmcm grade.
The value of the resistance R can be changed also by changing the distance between the polysilicon layer 13A and 13B.

[0012]Hereafter, the manufacturing method of this chip type silicon capacitor 1 is explained. (B) (A) of drawing 1, (B), (C), (D), and (A) of drawing 2 indicate the work process about the silicon wafer 11 to be to drawing 2 shows the work process in the chip after dicing of the silicon wafer 11.
[0013]First, for example, the silicon wafer 11 for IC is prepared and it forms in the surface (mirror plane side) of this silicon wafer 11 the SiO two-layer 12 which has a thickness of 5000 A by thermal oxidation. For example, the silicon wafer 11 after mirror polishing is oxidized thermally under an about 900 ** steam atmosphere, and the dielectric which consists of SiO two-layer 12 is formed on the surface. Although this thickness SiO two-layer [12] is determined according to the value of target pressure-proofing, it shall be 5000-6000 A preferably 1000-20000 A, for example. Etching removes the SiO two-layer generated at the rear face (non-mirror plane side) of this silicon wafer 11. (A) of drawing 1 shows this state.
[0014]Next, the polysilicon layer 13 is laminated on the surface of this silicon wafer 11 with a CVD method. This polysilicon layer 13 is an object for electrodes, for example, determines that area by patterning 5000 A of that thickness according to the electric capacity to need. As an electrode, it may replace with this polysilicon layer 13, and W-Si, Mo-Si, etc. may be used. This state is shown in drawing 1 (B).
[0015]After forming the photoresist 14 which has a rectangular window on the following **** and the polysilicon layer 13 (drawing 1 (C)), an etching process is performed to the polysilicon layer 13. As a result, as shown in drawing 1 (D), other polysilicon layers 13 are removed except for the polysilicon layers 13A and 13B used as an electrode.
[0016]Next, it forms SiO two-layer 15 at 5000 A in thickness with a CVD method on the polysilicon layers 13A and 13B and SiO two-layer [12]. And a predetermined window is

provided in the polysilicon layer 13A and the SiO two-layer 15 of 13B upper part by an etching process etc. (drawing 2 (A)). And the dicing process of common knowledge of the silicon wafer 11 in which two or more layers were laminated in this way cuts in a desired size, for example, the silicon chip 2 of a 2-mm mouth is formed. The lead 16 which becomes each of the polysilicon layers 13A and 13B on this silicon chip 2 from a Dumet wire etc. is welded by pressure. Thus, a silicon chip form capacitor is manufactured.

[0017]After welding the lead 16 by pressure to the polysilicon layers 13A and 13B, it may form SiO two-layer 15 so that the silicon chip 2 whole may be covered. It does not interfere with the surface of the polysilicon layers 13A and 13B by carrying out metal vacuum evaporation as composition which reduces the contact potential difference of the lead 16 and the polysilicon layers 13A and 13B. There may be two or more pairs of electrodes which consist of polysilicon layers without being restricted to a couple. Even if the number of an electrode is odd, it cannot be overemphasized that the electrode which certainly becomes a pair exists.

[0018]Drawing 4 is a sectional view of the chip type silicon capacitor 40 concerning the 2nd example of this invention. This chip type silicon capacitor 40 forms the conductive metal membranes 21, such as aluminum, in the rear face of the chip type silicon capacitor 40 concerning the 1st example of the above. If it is in this chip type silicon capacitor 40, the capacitor produced between the polysilicon layer 13A and the metal membrane 21, the capacitor produced between the polysilicon layer 13B and the metal membrane 21, and ** are formed. That is, it comes to connect the two above-mentioned capacitors to this silicon chip form capacitor 40 in series.

[0019]Drawing 5 is a sectional view of the chip type silicon capacitor 50 concerning the 3rd example of this invention. This chip type silicon capacitor 50 is provided with the capacitors C1-CN.

CR network circuit shown in the equivalent circuit of drawing 6 is constituted.

In drawing 5, SiO two-layer 12 is formed in the surface of the silicon chip 2, and two or more polysilicon layers 131-13N are formed on this SiO two-layer 12. The capacitor formed between the polysilicon layer 131 and the silicon chip 2 is equivalent to the capacitor C1 of drawing 6. Similarly, each capacitor formed between the polysilicon layers 132-13N and the silicon chip 2 is equivalent to the capacitors C2-CN. By changing suitably the area of the polysilicon layers 131-13N, it is possible to set the value of the capacitors C1-CN as a desired value.

[0020]And these polysilicon layers 131-13N are electrically connected by the metallic wiring 17, such as aluminum. The parasitic capacitance between the metallic wiring 17 and the polysilicon layer 2 is reduced by forming the oxide film 15 between such polysilicon layers 131-13N and metallic wiring 17. The doping layer 51 by which impurities, such as Lynn and boron, were doped - 5N+1 are formed in the prescribed position on the silicon chip 2. By changing suitably the doping layer 51 - the impurity concentration in each of 5N+1, it is possible to set

each doping layer 51 - the conductivity of 5N+1 as a desired value. Lead A and B are connected to the both ends of the silicon chip 2, and lead C is connected to the metallic wiring 17. These electrodes correspond to the terminal A, B, and C of drawing 6.

[0021]Therefore, if it is in the chip type silicon capacitor 50 constituted in this way, it can be set as the value of the capacitors C1-CN, the resistance R1 - a request of the value of RN+1. Therefore, it becomes possible to use RC network circuit shown in the equivalent circuit of drawing 6 as a low pass filter of arbitrary cut off frequencies. The Chebyshev form or the filter of the Bata Wace type is also realizable by changing suitably the capacitors C1-CN, the resistance R1 - the value of RN+1.

[0022]It is also possible by forming metallic wiring on a spiral on the silicon chip 2 to realize LC network circuit. In this case, this chip type silicon capacitor 50 can also be operated as a delay line.

[0023]

[Effect of the Invention]setting to a chip type silicon capacitor according to this invention, as stated above -- any of two electrodes -- although -- since one field of the silicon chip laminates via silicon oxide, it becomes possible from one field of a silicon chip to pull out both leads. Therefore, since leading about of a circuit pattern can be shortened when it mounts this chip type silicon capacitor in a substrate etc., it becomes possible to prevent the high frequency characteristic of a circuit from getting worse.

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TECHNICAL FIELD

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PRIOR ART

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EFFECT OF THE INVENTION

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MEANS

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OPERATION

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